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Dependences of Electrical Properties of Thin GeSbTe and AgInSbTe Films on Annealing

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We studied the electrical properties of 20- and 50-nm-thick $Ge_2Sb_2Te_5$ and AgInSbTe films for nonvolatile lateral transistor memory devices. Both kinds of thin films were prepared as film samples and device samples which were then annealed at temperatures from 140 to 415°C. It is known that crystal size can be effectively reduced with film thickness on the basis of X-ray diffraction analysis. The resistances of all film samples annealed at 140–415°C decreased by approximately 5–6 orders of magnitude. In the case of device samples, however, the source-drain resistances of $Ge_2Sb_2Te_5$ samples were first reduced and then reversely increased and it seemed that the resistances of AgInSbTe samples did not drop. The abnormal resistance increase above the crystallization temperature may be caused by phase change and thermal expansion, as we analyzed in this paper. Finally, the resistance changes of device samples with channel lengths in the range of 0.4–3 μm were discussed from the point of view of miniaturizing the phase change memory device. [DOI: 10.1143/JJAP.44.6208]

KEYWORDS: transistor memory, phase change, chalcogenide, $Ge_2Sb_2Te_5$, AgInSbTe, X-ray diffraction, electrical properties and annealing

1. Introduction

Chalcogenides have been noted as suitable phase change (PC) memory materials for nonvolatile memory devices by many researchers.[1,2] To increase memory capacity and reduce power consumption, the active area of memories has been shrunk to nanometer scale.[3]

We proposed a PC channel transistor memory based on the combination of phase change effect for nonvolatile memory and Coulomb blockade effect at room temperature for the selection of memory cells. We demonstrated the possibility of realizing a one-transistor memory cell using 50-nm-thick $Ge_2Sb_2Te_5$ (GST) with a channel length of 3 μm.[4]

It has been suggested that the crystallite size of the PC channel when in the polycrystalline state should be smaller than 10 nm in diameter for the Coulomb blockade effect to occur at room temperature.[5] Hence, it is necessary to study thin films and small memory structures using GST and AgInSbTe (AIST) to realize the further miniaturization of memory elements for ultrahigh-density memories. Friedrish *et al.* investigated structural transformations of GST films by electrical resistance measurements and X-ray diffraction (XRD) analysis.[6] However, the films used were as thick as 80 and 200 nm. In this investigation 20- and 50-nm-thick films were studied as film samples and device samples with a channel length of 0.4–3 μm connected by source and drain electrodes for very small PC memory devices.

2. Experimental

We prepared 20- and 50-nm-thick GST and AIST films on glass (film samples) and the films for channels on a Si_3N_4 layer (device samples) simultaneously using a sputtering system (i Miller: Shibaura Mechatronics). The deposition rate was approximately 0.57 nm/s. These samples were then annealed at temperatures in the range from 140 to 415°C in N_2 for 10 min. The crystal structures of GST films formed by annealing were first characterized using X-ray diffractometer (RINT 2000: Rigaku) in which Cu Kα (wavelength of X-ray $\lambda = 0.15418$ nm) was used. Then, the current–voltage (I–V) characteristics of the both film and device samples were measured using a semiconductor parameter analyzer (4155B: Agilent Technologies) in air at room temperature. In the I–V measurements, tungsten (W) probes were used to contact the samples.

3. Results and Discussion

3.1 XRD patterns of film samples

A schematic diagram of the film samples is shown in Fig. 1. The sample fabrication began with a glass substrate and a layer of chalcogenide and a capping layer of 10-nm-thick $ZnS–SiO_2$ were then sputtered.

Figure 2 shows XRD patterns of 20- and 50-nm-thick GST thin films, for which the backgrounds were removed. No peaks could be observed for the films annealed at 140°C, which means that the films were amorphous. The 50-nm-thick GST films annealed at 180 and 258°C are identified as having a face-centered cubic (FCC) crystal structure and their lattice constant a is determined to be 0.60203 nm on the basis of an analysis of peak positions. A new peak appeared at 28.94° for the 50-nm-thick films annealed at 338 and 415°C. It is the peak $(10\bar{3})$ that corresponds to a hexagonal structure and other newly appeared peaks indicate that the FCC crystal structure was transformed to a hexagonal structure.[6] However, such a peak $(10\bar{3})$ is not obvious in the case of 20-nm-thick films annealed at 338°C. Consequently, the critical temperature of the 50-nm-thick films for the transition from FCC to the hexagonal structure may be lower than that of the 20-nm-thick films.

Crystallite size can be estimated using the Scherrer's equation

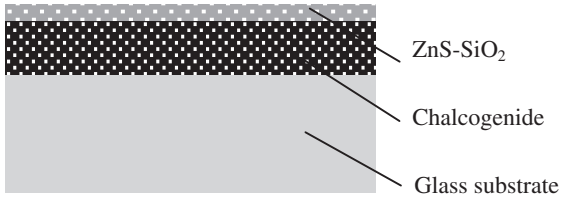

Fig. 1. Schematic cross section of film samples.

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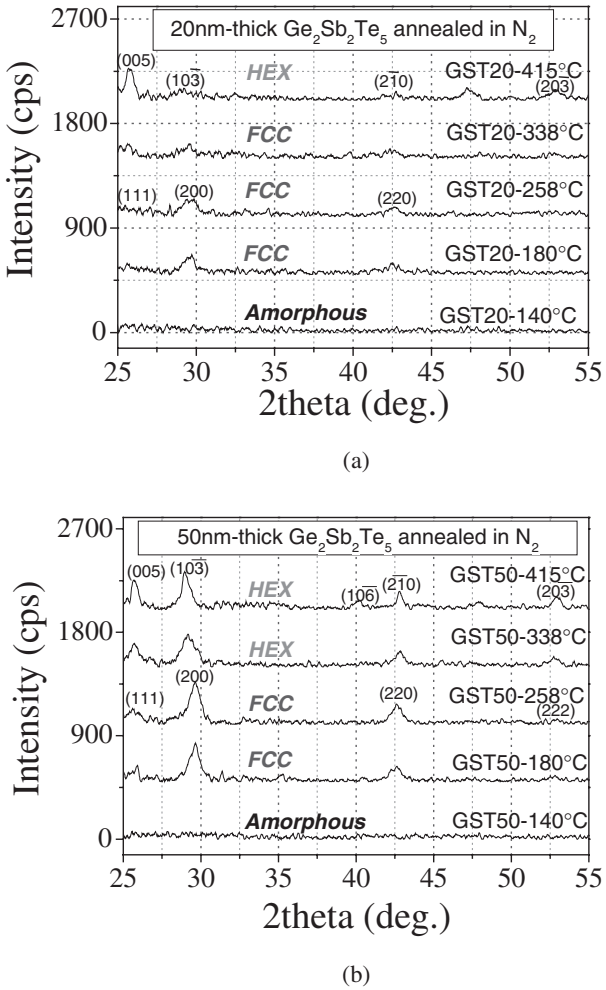


Fig. 2. XRD patterns of (a) 20-nm- and (b) 50-nm-thick $Ge_2Sb_2Te_5$ films annealed at different temperatures.

$$L_{hkl} = \frac{0.89\lambda}{\beta_{hkl}\cos\theta}, \tag{1}$$

where L_{hkl} is the mean crystallite size, λ is the wavelength of X-rays, β_{hkl} is the full-width at half maximum (FWHM) intensity of the peak in radians and θ is the diffraction angle of the peak.[7] The subscript *hkl* is the Miller index of the crystal plane. The mean crystallite sizes are 9.4 and 11.3 nm according to the analysis of the (220) peaks of the 20- and 50-nm-thick GST films annealed at 258°C. Consequently, we can successfully refine the crystal to some extent by reducing the film thickness.

The transition temperatures $T_{A\rightarrow FCC}$ from amorphous to FCC crystalline and $T_{FCC\rightarrow HEX}$ from FCC to hexagonal as well as mean crystallite sizes based on XRD patterns in Fig. 2 are summarized in Table I.

Table I. Transition temperatures and mean crystal sizes according to XRD patterns shown in Fig. 2.

	20-nm-thick GST	50-nm-thick GST
$T_{A\rightarrow FCC}$ (°C)	140–180	140–180
$T_{FCC\rightarrow HEX}$ (°C)	338–415	258–338
Mean crystal size (nm)	9.3	11.4

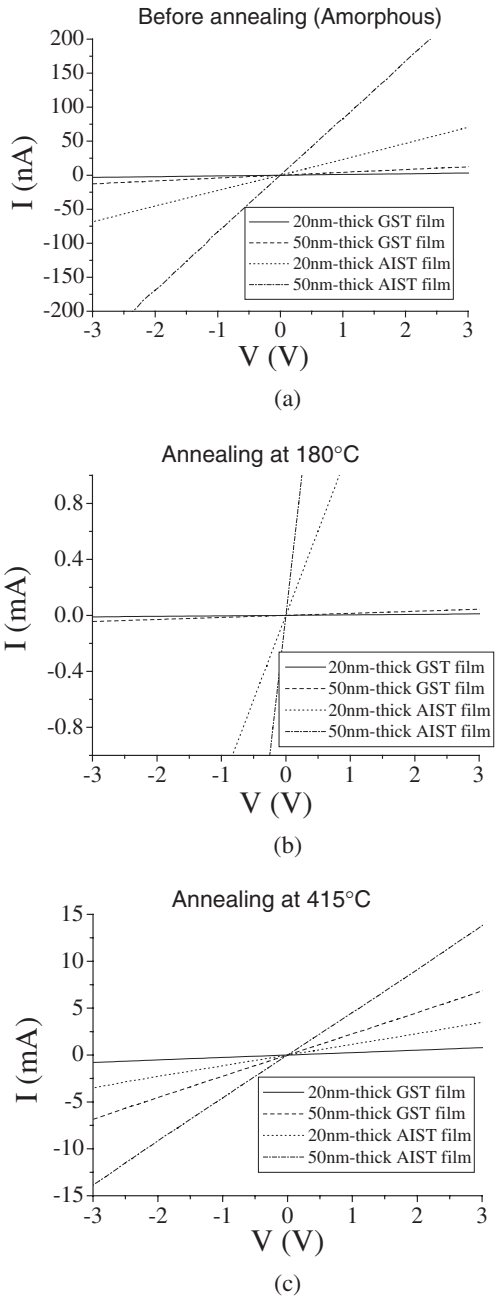


Fig. 3. *I–V* characteristics of GST and AIST films (a) before annealing, (b) after annealing at 180°C, and (c) after annealing at 415°C.

3.2 Annealing temperature dependence of electrical properties for film samples

The *I–V* characteristics of the films were measured in the range from −3 to 3 V by fixing the separation between two probes as shown in Fig. 3. The characteristics are linear, which indicates ohmic contact between the W probes and chalcogenide films.

The changes in resistance of the film samples with annealing temperature calculated from the *I–V* curves will be described for three regions labeled as A, B, and C in Fig. 4.

3.2.1 Below 140°C (amorphous, region A in Fig. 4)

The resistances of 20-nm-thick samples of both GST and AIST decrease a little at the lowest annealing temperature of 140°C. GST and AIST films were sputtered by setting the

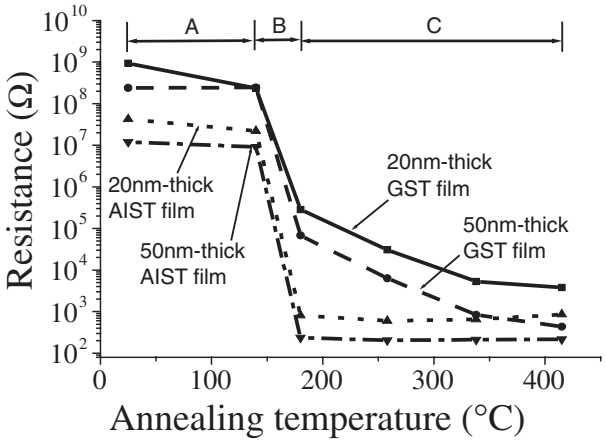


Fig. 4. Annealing temperature dependences of resistance of GST and AIST films.

substrate temperature at room temperature (about 25°C) and the as-deposited GST and AIST films should all be initially amorphous. We consider that crystallization of the films in fact includes both heterogeneous nucleation and crystal growth. The detected drop in resistance of the thinner films indicates that initial fine nucleuses formed. Therefore, the crystallization incubation temperature, i.e., fine nucleus formation temperature might become low with decreasing film thickness. This phenomenon could be understood from the viewpoint of heterogeneous nucleation, which occurs under most real crystallization conditions. Since a much lower energy is required to form nucleus at the existed impurities, wall, or other interfaces, nucleuses might preferentially form at these sites. In the film samples, the chalcogenide film contacts both the underlying substrate and the capping layer, so the contact area where heterogeneous nucleuses preferentially form is $2A$ for a certain film area A. For a chalcogenide film with a thickness of t, the ratio of contact area $2A$ to volume V ($= A \times t$) is $2/t$. This indicates that for a given volume, the contact area for a thin chalcogenide film is larger than that for a thick film. In other words, heterogeneous nucleation is easier for a thin film due to its large interface area, which therefore leads to its lower crystallization incubation temperature.

3.2.2 *From 140 to 180°C (crystallization, region B in Fig. 4)*

The resistances of AIST films drop rapidly from several 10^7 to $10^2\,\Omega$ due to crystallization. On the other hand, resistances of the GST films drop in a narrower range from several 10^8 to $10^5\,\Omega$ due to crystallization to the FCC structure (see XRD patterns).

3.2.3 *Above 180°C (crystalline, region C in Fig. 4)*

The resistances of AIST films saturate, that is, they remain constant, indicating almost complete crystallization in this range. On the other hand, the resistances of the GST films gradually further decrease above 180°C.

On the basis of the difference in resistance change after crystallization between AIST and GST films, it thus seems that the AIST material is very suitable for binary storage and the GST material is suitable for multilevel storage realized by adopting different resistance values.

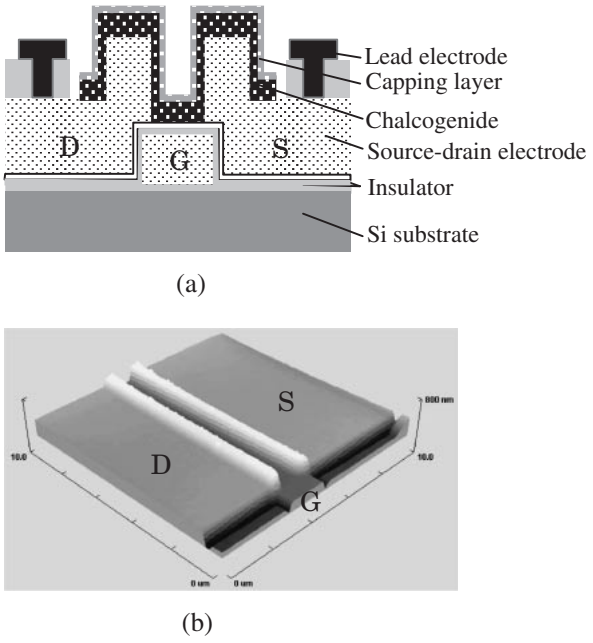


Fig. 5. (a) Schematic cross section of device sample. (b) The three-dimensional AFM image of 20-nm-thick AIST device sample.

3.3 *Annealing temperature dependences of electrical properties for device samples*

A schematic diagram of the lateral device samples is shown in Fig. 5(a). Figure 5(b) shows an atomic force microscopy (AFM) image of an AIST device sample.

Figure 6 shows I–V characteristics of the device samples before and after annealing in the range from -2 to 2 V. All of the characteristics are nonlinear, indicating that there existed Schottky contact between the electrodes and the chalcogenide channel.

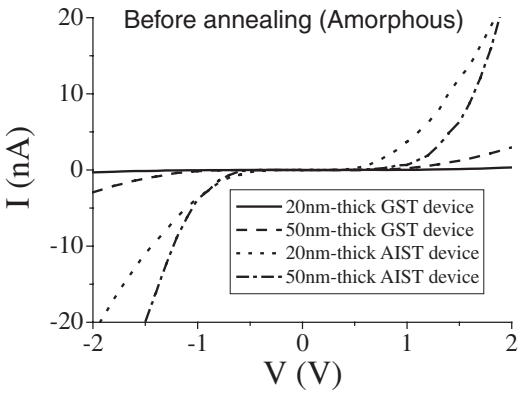
The resistances of the device samples have been roughly calculated at a voltage of 2 V from Fig. 6. The measured resistance of device samples R in fact is composed of contact resistances $R_{\text{Si-ch}}$ (from Si to chalcogenide) and $R_{\text{ch-Si}}$ (from chalcogenide to Si) and the resistance of the phase change chalcogenide film channel R_{ch}. It can be expressed as

$$R = R_{\text{Si-ch}} + R_{\text{ch-Si}} + R_{\text{ch}}. \tag{2}$$

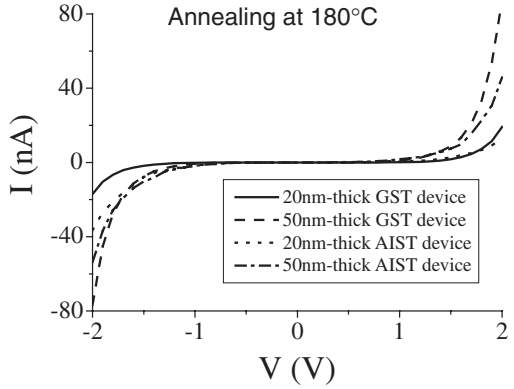
The resistances of the GST device samples have a similar trend to those of the film samples annealed below 258°C. Above 258°C, the resistances increase reversely. On the other hand, the resistances of the AIST devices decrease a little at 140°C and then increase. If there is no influence of contact resistances, the resistance changes of the device samples should have the same trend as those of the film samples. The difference in resistance change between the film and device samples may be thus caused by stress due to phase change and thermal expansion in device samples. From the resistance changes with temperature, only GST device samples annealed at below 258°C are suitable for the study of electrical properties.

Next, an analysis of stress caused by phase change and thermal expansion in the elastic range will be given below, which is illustrated in Fig. 7.

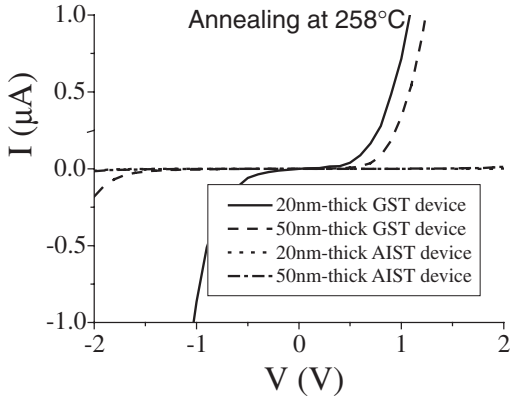
The PC film is so thin that we can analyze the device samples according to plane stress. Thermal stress in the thin PC film σ_{Tf} can, therefore, be expressed as



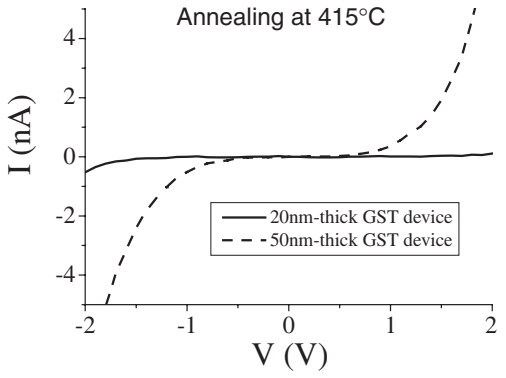
(a)



(b)



(c)



(d)

Fig. 6. *I–V* characteristics of GST and AIST devices with a channel width of 9 μm and a channel length of 3 μm (a) before annealing, (b) after annealing at 180°C, (c) after annealing at 258°C and (d) after annealing at 415°C. *I–V* characteristics of the AIST devices annealed at 415°C could not be obtained due to their high resistances.

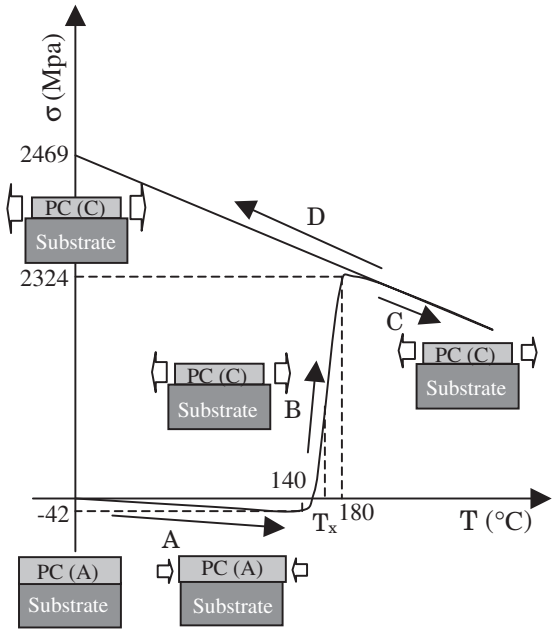


Fig. 7. Schematic diagram of stress in the GST device samples as a function of temperature in the elastic range.

$$\sigma_{\mathrm{Tf}} = \frac{E_{\mathrm{f}}}{1-\nu_{\mathrm{f}}}(\alpha_{\mathrm{Ts}} - \alpha_{\mathrm{Tf}})\Delta T, \tag{3}$$

where $E_{\mathrm{f}}/1-\nu_{\mathrm{f}}$ is biaxial modulus of the film Y_{f}, E_{f} is Young's modulus, ν_{f} is Poisson's ratio, α_{Tf} and α_{Ts} are the linear coefficient of thermal expansion (CTE) of the PC material and CTE of the substrate, and ΔT is the temperature change. Consider the PC film initially unstressed and in the amorphous state, σ_{Tf} is minus and the PC film will thus be subjected to a compressive stress as the device is heated to a temperature below the crystallization temperature T_{x} (Process A in Fig. 7). For the crystallization process (Process B in Fig. 7), stress induced by phase change can be given by

$$\sigma_{\mathrm{pc}} = -\bar{Y}_{\mathrm{f}}\varepsilon_{\mathrm{pc}}, \tag{4}$$

where $\bar{Y}_{\mathrm{f}}$ is the average biaxial modulus of the amorphous and crystalline PC film and $\varepsilon_{\mathrm{pc}}$ is the strain caused by phase change. After crystallization takes place in the PC material, the PC material should be subjected to a tensile stress, given that the contraction caused by phase change is much larger than thermal expansion below T_{x}. If we further heat the device to a higher temperature (Process C in Fig. 7), the tensile stress then decreases according to eq. (3). Finally, after we cool the device to room temperature (Process D in Fig. 7), the PC film is subjected to a higher tensile stress.

The stress values for the GST samples shown in Fig. 7 are based on the above analysis and the physical properties listed in Table II. The stress values seem high since we analyzed the stress only in the elastic range. A large tensile stress, as a result, arises from phase change and thermal expansion after crystallization in devices when the sample is cooled to room temperature. If the tensile stress exceeds the allowable stress, a failure of contact between electrodes and the PC film could take place.

Furthermore, for example, let us look at Fig. 6(d) again, in which the resistance after annealing at 415°C was even near

Table II. Reported physical properties of phase change materials and an insulator material.[8–10]

Alloy	State	Y_f (GPa)	α (10^{-6} K^{-1})	Strain induced by crystallization (%)
$Ge_2Sb_2Te_5$	Amorphous	27.6 (±4.7)	16.8 (±2.6)	−6.5
	Crystalline	45.2 (±8.2)	24.4 (±3.8)	
AgInSbTe	Amorphous	10.5 (±2.2)	34.4 (±12.9)	−5.5
	Crystalline	22.6 (±4.8)	32.6 (±7.5)	
Si_3N_4	—	—	3.69	—

to that before annealing. On the basis of the above analysis, most of crystals and parts of the amorphous region which formerly contact the electrodes very well might peel from the electrodes due to large tensile stress after annealing. If so, the contact resistances $R_{Si\text{-}ch}$ and $R_{ch\text{-}Si}$ should increase significantly although many of the low-resistance crystals formed in the phase change film between electrodes, and R_{ch} after annealing at 415°C might drop to about 10^{-5} of that before annealing according to Fig. 4. So on the basis of eq. (2), the measured resistance after annealing at a higher temperature might be near to or even larger than that before annealing.

To investigate the structure size dependences of the electrical properties of the devices, we measured the resistances of 50-nm-thick GST devices with a channel width of 9 μm and a channel length in the range of 0.4–3.0 μm. Two of these results are shown in Fig. 8. Similar resistance changes for the two devices could be observed. As a result, shrinking the channel length while maintaining a constant channel width of 9 μm might have a weak influence on the electrical properties. The source–drain resistance of the device with a channel length of 0.4 μm should be 1/5 of that of the device with a channel length of 2 μm. The measured results, however, disagree with this simple prediction. The cause of the disagreement remains unclear at present. The weak channel length dependence cannot be caused by the leakage current through the gate insulator. The reason is that the gate insulator (30-nm-thick Si_3N_4 and 30-nm-thick SiO_2) is sufficiently thick to suppress the leakage current between source and drain and gate electrodes. In experimental results, the leakage current through the gate insulator was not observed even when the voltage drop between the gate and source or drain electrode is as high as 40 V. We will investigate the influence of the channel width on the electrical properties of the device in a future study.

4. Conclusions

We studied the fundamental properties of phase change materials for ultrahigh-density nonvolatile lateral transistor memories. According to XRD patterns of GST films and the electrical properties of GST and AIST films and devices, the following conclusions (1)–(3) and (4)–(6), respectively, could be drawn.

(1) The crystallization temperature is in the range of 140–180°C and the transformation temperature from a FCC to a hexagonal structure for 50-nm-thick GST films is in the range of 258–338°C. However, 20-nm-thick GST films might have a higher critical temperature for the transformation from a FCC to a hexagonal structure.
(2) The lattice constant of the FCC crystal structure of GST films was determined as 0.60203 nm.
(3) The mean crystal sizes of GST films could be effectively reduced with film thickness.
(4) The crystallization incubation temperatures in both GST and AIST films tend to be shifted to a lower temperature with decreasing thickness.
(5) The disagreement of resistance changes of the device samples with those of the film samples may result from stress induced by phase change and thermal expansion in the device samples.
(6) There is a weak influence of the channel length above 0.4 μm on the electrical properties of the device samples.

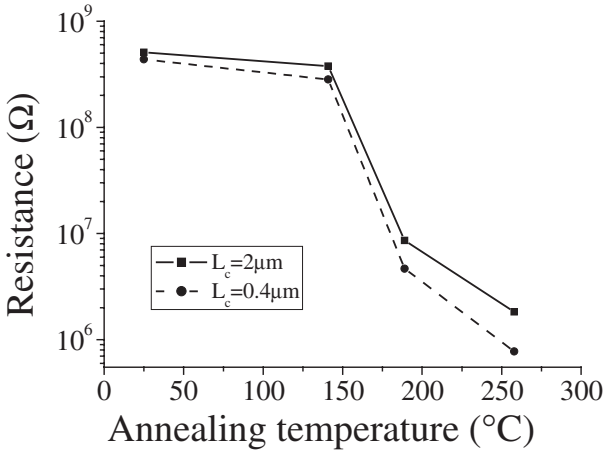


Fig. 8. Annealing temperature dependences of resistance of 50-nm-thick GST devices with channel lengths of 2.0 and 0.4 μm.

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